

JE200 and JE210 JPEG Encoder

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Product Specification



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Core Facts	
Provided with core	
Documentation	Programmers Manual
Design File Formats	NGC netlist
Verification	Testbench, Testvectors
Constraints File	Not needed
Instantiation Template	VHDL
Reference design & application notes	Demo Application
Additional Items	
Simulator Tool Used	
ModelTech ModelSim 5.7c	
Support	
Penz VHDL	

Features

- Optimized for Xilinx FPGA
- Block building RAM included, no external RAM needed
- Compliant with Baseline ISO/IEC 10918-1
- Motion-JPEG capability
- Monochrome or Color (YCbCr 4:2:2)
- Up to 4096 pixel per row
- Baseline encoder
- 8-bit/pixel input
- Line by line pixel input
- 2 Quantization tables, reprogrammable
- 4 fixed Huffman tables (two DC and two AC)
- Fully synchronous design
- Fully stall able design
- Single clock cycle per pixel encoding
- No pause cycles between blocks

Applications

The JE200 and JE210 are designed as coprocessor for a CPU to speed up the baseline encoding of a pixel stream to a JPEG encoded data stream. They are suitable where an image must be compressed in real-time, like in Frame grabbers, intelligent cameras, surveillance systems and scanners.

The JE200 is optimized for Virtex, Virtex-E, Spartan-II and Spartan-IIe devices.

The JE210 is optimized for Virtex-II, Virtex-IIP and Spartan-III devices.

Table 1: Core Implementation

Supported Family	Device Tested	Mode	Flip Flops	4 input Luts	Block RAM	Hard mult.	TBufs	IOBs	Performance	Xilinx Tools
Spartan-IIe	XC2S600E-6	2048 color	2159	4158	65	--	192	54	70 MHz	ISE 6.1
Spartan-IIe	XC2S600E-6	512 mono	2156	4074	9	--	136	54	70 MHz	ISE 6.1
Spartan-III	XC3S2000-4	2048 color	1775	2818	17	16	--	54	90 MHz	ISE 6.1
Virtex-II	XC2V1000-4	1024 color	1771	2917	9	16	--	54	95 MHz	ISE 6.1

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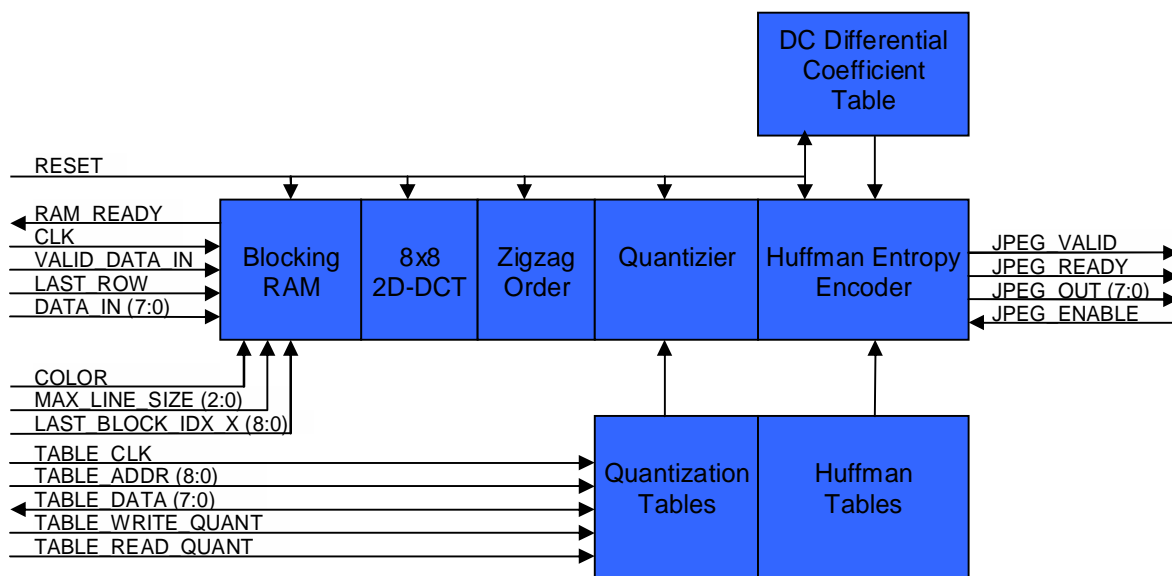
General Description

The JE200 encodes a monochrome or color (YCbCr 4:2:2) image into a JPEG standard conform bit stream. With build in RAM, to rearrange the lines into the 8x8 pixel blocks. Baseline encoding with a pixel size of 8 bit is used. The bit stream appears on the 8 bit output register. The core is stall able by the handshake signals on the pixel input and the bit stream output interface. No Marker is generated, so the designer has the choice to generate the header with a CPU or use a fixed table. Sample header and a C++ class to generate the header are delivered with the core. Standard DC- and AC-tables for quantization and Huffman encoding are predefined. The content of the Quantization tables can be reprogrammed.

Functional Description

The incoming lines are stored into the internal RAM and read out in 8x8 pixel blocks. The block goes through the two-dimensional discrete cosine transformation (2D-DCT) and will be transformed into 64 coefficients into the frequency domain. Now, the coefficients will be read out in a Zigzag order and quantized by dividing through the selected Quantization table. The first (DC) quantized coefficient is differentially coded, using the most recently DC coefficient from the same component. Now all coefficients are run length coded to Run-Size symbols. Finally the symbols are Huffman coded, using the code from the selected Huffman table. The bit-stream of Huffman codes is divided into parts with 8 bit and stored in the output register.

Figure 1: Encoder Block Diagram



Core Modifications

Usually no core modifications are necessary, but when a special interface or more tables are needed, modifications can be applied. Please contact Penz-VHDL for more information.

Verification Methods

The encoder has been validated as functional and timing simulation with several test patterns under ModelSim XE 5.7c. A final verification has been done in a demo-application with some color and BW images.

Pinouts

Table 2: Core Signal Pinout

Signal Name	Direct.	Description
Pixel Input Interface		
CLK	In	Encoder clock
RESET	In	Reset encoder state machines
VALID_DATA_IN	In	Pixel is valid
DATA_IN (7 : 0)	In	Pixel input
LAST_ROW	In	Last row in this image
COLOR	In	Mode mono chrome or color
MAX_LINE_SIZE (2:0)	In	Number of samples per row
LAST_BLOCK_IDX_X (8:0)	In	Index of the last 8 pixel-block in a row
RAM_READY	Out	Encoder is ready for new pixel
Compressed Data Output Interface		
JPEG_ENABLE	In	Data handshake
JPEG_VALID	Out	Output data is valid
JPEG_READY	Out	Last data for this field
JPEG_OUT (7:0)	Out	Output data
Tables Programming Interface		
TABLE_CLK	In	Clock for table reprogramming
TABLE_ADDR (8:0)	In	Table select and addressing
TABLE_DATA (7:0)	In/Out	Table read- or write-data
TABLE_WRITE_QUANT	In	Write data into Quantization table
TABLE_READ_QUANT	In	Read data from Quantization table

Recommended Design Experience

Only basic VHDL knowledge is necessary, no manual placement is required. Advanced designers can reach a higher performance.

Ordering Information

The JPEG Encoder core is provided under license by Penz-VHDL. The VHDL source code is also available. Please contact Penz-VHDL for information about pricing and conditions of sale.