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## JE440 Multiple Channel JPEG Encoder for Altera Stratix and Stratix II FPGAs

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Product Specification V0.9

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Penz VHDL  
Frankenstraße 16  
D-55299 Nackenheim  
Germany

Phone: +49 (0)6135-950328  
Fax: +49 (0)6135-950329  
E-Mail: mail@penz-vhdl.de  
URL: www.penz-vhdl.de

### Features

- Parallel compression of 4 unsynchronized images
- Optimized for Altera Stratix and Stratix II FPGAs
- Marker generation included
- Block building RAM included, no external RAM needed
- JPEG file output
- Compliant with Baseline ISO/IEC 10918-1
- Motion-JPEG capability
- Monochrome or Color (YCbCr 4:2:2)
- Up to 2048\* samples per row
- Baseline encoder
- 8-bit/sample input
- Line by line sample input
- 2 Quantization tables, reprogrammable
- 4 fixed Huffman tables (two DC and two AC)
- Fully synchronous design
- Single clock cycle per sample encoding

Core Facts	
Provided with core	
Documentation	Programmers Manual
Design File Formats	netlist
Verification	Testbench, Testvectors
Constraints File	Not needed
Instantiation Template	VHDL
Reference design & application notes	Demo Application
Additional Items	
Simulator Tool Used	
ModelTech ModelSim 6.0	
Support	
Penz VHDL	

### Applications

The JE440 is designed to generate four baseline encoded (Motion) JPEG files from four different images, in real-time and without using a CPU. There is no need to synchronize the video sources also the image size need not to be the same. The resource count of the JE440 is only the half of four single encoder instances. It is suitable where multiple images must be compressed in real-time, like in Frame grabbers, intelligent cameras and surveillance systems.

**Table 1: Core Implementation**

Device	Samples per Row	Logic Elements	M512 RAMs	M4K RAMs	M RAMs	DSP Elements	IOBs	Performance
EP1S25-C8	2048*	6800	20	32	1	24	221	27 MHz <sup>+</sup>
EP1S25-C5	2048*	6800	20	32	1	24	221	39 MHz <sup>+</sup>
EP2S30-C5	2048*	6700	20	32	1	24	221	51 MHz <sup>+</sup>
EP2S30-C3	2048*	6700	20	32	1	24	221	62 MHz <sup>+</sup>

\* Contact us for more samples per row.

<sup>+</sup> Maximal sample clock, the encoder clock is four times higher.

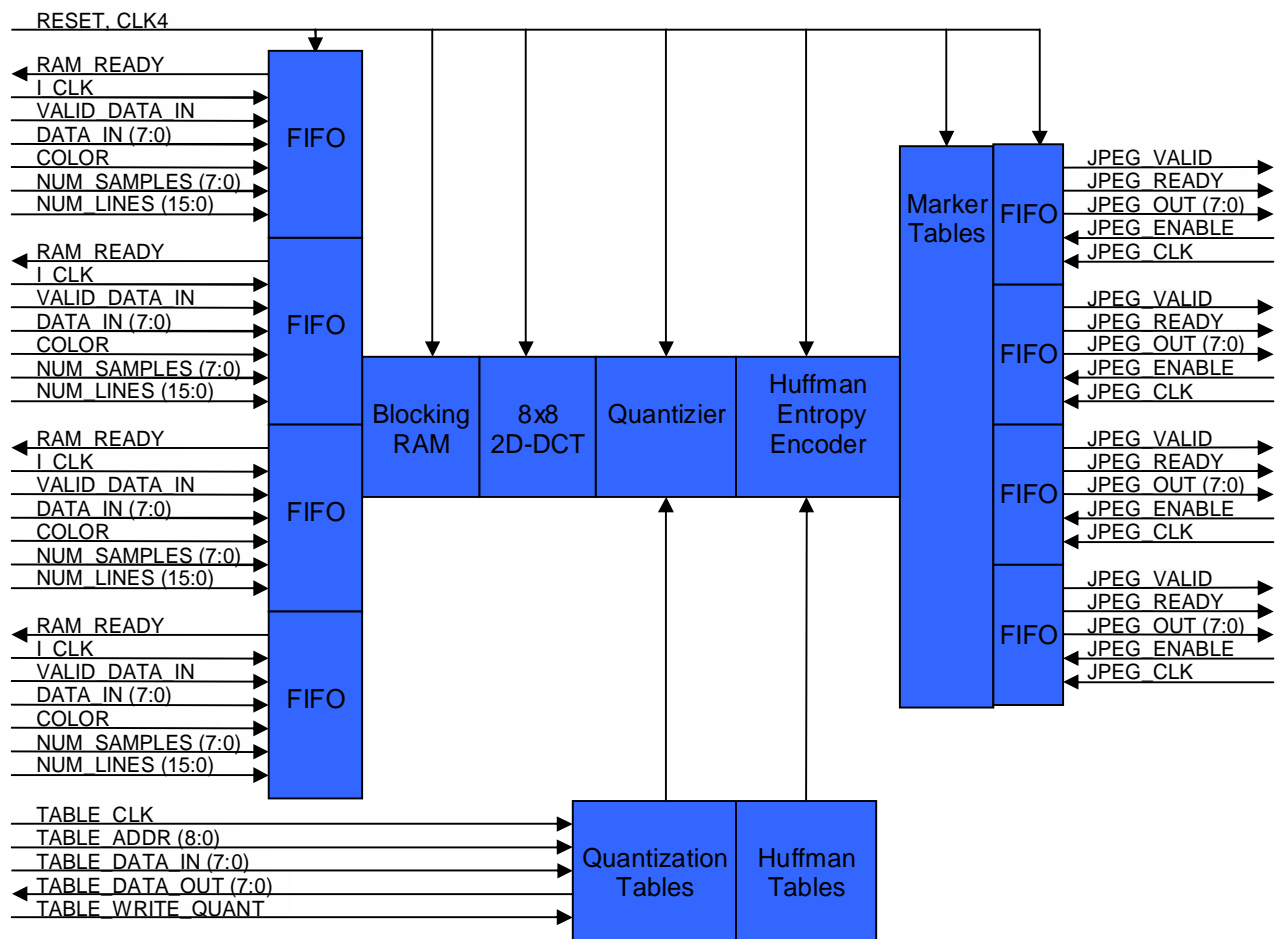
## General Description

The JE440 encodes up to four monochrome or color (YCrCb 4:2:2) images into four JPEG standard conform bit streams. With built in RAM, to rearrange the lines into the 8x8 sample blocks. Baseline encoding with a sample size of 8 bit is used. All needed Markers are generated too. The complete JPEG files appear on the four 8 bit output registers. The core is stall able by the handshake signals on the sample input and the file output interface. Standard DC- and AC-tables for quantization and Huffman encoding are predefined. The content of the Quantization tables can be reprogrammed.

## Functional Description

The incoming lines are stored into the internal RAM and read out as 8x8 samples blocks. The blocks go through the two-dimensional discrete cosine transformation (2D-DCT) and will be transformed into 64 coefficients into the frequency domain. Now, the coefficients will be read out in a Zigzag order and quantized by dividing through the selected Quantization table. Each channel has its own set of Quantization tables. The first (DC) quantized coefficient is differentially coded, using the most recently DC coefficient from the same component. Now all coefficients are run length coded to Run-Size symbols. Finally the symbols are Huffman coded, using the code from the Huffman table. The bit-stream of Huffman codes is divided into parts with 8 bit and embedded between all needed Markers to generate a valid JPEG file.

Figure 1: Encoder Block Diagram



## Core Modifications

Usually no core modifications are necessary, but when a special interface or more tables are needed, modifications can be applied. Please contact Penz-VHDL for more information.

## Verification Methods

The encoder has been validated as functional and timing simulation with several test patterns under ModelSim 6.0. A final verification has been done in a demo-application with some color and BW images.

## Pinouts

Table 2: Core Signal Pinout

Signal Name	Direct.	Description
<b>Control interface</b>		
RESET	In	Encoder reset
CLK4	In	Encoder clock
<b>Sample input interface, four times for each channel</b>		
I_CLK	In	Sample input clock
VALID_DATA_IN	In	Sample is valid
DATA_IN (7 : 0)	In	Sample input
COLOR	In	Mode, mono chrome or color
NUM_SAMPLE (7:0)	In	Number of samples per line in 8 units
NUM_LINES (15:0)	In	Number of lines per image
RAM_READY	Out	Encoder is ready for new sample
<b>Compressed data output interface, four times for each channel</b>		
JPEG_CLK	In	Clock for JPEG file output
JPEG_ENABLE	In	Data handshake
JPEG_VALID	Out	Output data is valid
JPEG_READY	Out	Last data for this field
JPEG_OUT (7:0)	Out	Output data
<b>Tables programming Interface</b>		
TABLE_CLK	In	Clock for table reprogramming
TABLE_ADDR (8:0)	In	Table select and addressing
TABLE_DATA_OUT (7:0)	Out	Table read data
TABLE_DATA_IN (7:0)	In	Table write data
TABLE_WRITE_QUANT	In	Write strobe for Quantization table

## Recommended Design Experience

Only basic VHDL knowledge is necessary, no manual placement is required. Advanced designers can reach a higher performance.

## Ordering Information

The JPEG Encoder core is provided under license by Penz-VHDL. The VHDL source code is also available. Please contact Penz-VHDL for information about pricing and conditions of sale.